DETAILED ACTION

Response to Arguments

Applicant's arguments, see Pre-Brief conference request filed 11/19/09, with respect to the rejection(s) of claim(s) 1-7, 10-17 under 35 USC 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Moroney, US Patent No. 6711684

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1-7 and 10-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzales, US Patent No. 5488688, and further in view of Moroney, Us Patent No. 6711684

2. As per claims 1 and 11, Gonzales teaches:

A processor operable in a plurality of modes, and a plurality of domains, said plurality of domains comprising a first domain and a second domain, the processor comprising:

monitoring logic configured to perform a debug or trace function to monitor said processor and to capture diagnostic data in response to performing said debug or trace function;

> *[see fig. 1] element 23 is viewed as the claimed "monitoring logic", element 21 is viewed as the claimed "processor", and element 24 is viewed as the "debug function".*

a storage element operable to contain at least one control parameter;

[see col. 3, lines 29-32]

control logic operable to control said monitoring logic in dependence on said at least one control parameter and the domain in which said processor is operating, to suppress capturing of diagnostic data relating to predetermined activities of said processor in said first domain.

[see col. 3, lines 34-39]

Gonzales is mute in teaching that the processor is operable to operate in two different domains nor does Gonzales teach that while diagnostic data capture is being suppressed in one domain, capturing of diagnostic data in the second domain is allowed. For this limitation, examiner relies on the Moroney reference.

Moroney teaches a method for storing information in a processing device with flexible security. The method receives a two separate downloads via different download paths. the first plaintext is stored and then when the second download, a key, is downloaded, the first download path is disabled and the second path is utilized to store the secure information (see col. 2, lines 11-32). Examiner views the two paths as the claimed "first and second domains". Moroney further teaches at col. 4, lines 16-38, that the structure of the paths allows of multi-level security if the processing device (unrestricted, partially restricted, and fully restricted). It would have been obvious to one of ordinary skill in the art to modify the Gonzales reference to include the limitation of operating in two domains and allowing data capture in one domain while suppressing it in another domain so that non-sensitive data can be stored in an area separate from secure data in order to make the system not susceptible to attack by pirates (Moroney, col. 1, lines 55-63).

As per claims 2 and 12, Gonzales teaches:

A processor according to claim 1, wherein the first domain is a secure domain and the second domain is a non-secure domain, said processor being operable such that when executing a

program in a secure mode within said secure domain said program has access to secure data which is not accessible when said processor is operating in a non-secure mode within said non-secure domain.

[see column 3, lines 40-53, wherein the cited first mode is viewed as the non-secure mode and the cited second mode is viewed as the secure mode.]

As per claims 3 and 13, Gonzales teaches:

A processor according to claim 1, wherein the at least one control parameter provides an indication of said domain of operation of the processor, said control logic being operable to suppress capturing of diagnostic data when said processor switches from second to first domain.

[see col. 3, lines 34-39, wherein the cited signal is viewed to be analogous to the claimed "control parameter".]

As per claims 4 and 14, Gonzales teaches:

A processor according to claim 1, wherein said at least one control parameter identifies an application, said control logic being operable to suppress capturing of diagnostic data when said processor switches from an identified application in said first domain to an application in said first domain not identified by said at least one control parameter.

[see column 4, lines 30-38]

As per claims 5 and 15, Gonzales teaches:

A processor according to claim 1, wherein said first domain comprises a plurality of modes and said at least one control parameter identifies a particular mode within said first domain, said control logic being operable to suppress capturing of diagnostic data when said processor switches between an identified mode within said first domain and a mode within said first domain not identified by said at least one control parameter.

[see column 3, lines 40-53]

As per claims 6 and 16, Gonzales teaches:

A processor according to claim 5, wherein said plurality of modes in said first domain comprise a user mode and a privileged mode.

[see rejection of claim 2, wherein the first mode is a user mode and the second mode is a privileged mode.]

As per claims 7 and 17, Gonzales teaches:

A processor according to claim 1, wherein said control logic is operable to control said monitoring logic to resume capturing of diagnostic data when said processor switches back from said predetermined activity to an activity for which capturing of diagnostic data is not suppressed.

[see column 3, lines 60-65, and col. 4, lines 1-3]

As per claim 10, Gonzales teaches:

A processor according to claim 1, wherein said control logic suppresses capture of said diagnostic data by removing power input to the monitoring logic.

[see column 6, lines 41-55]

*. Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulaney Street
Alexandria, VA 22314

*. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel L. Hoang whose telephone number is 571-270-1019. The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser Moazzami can be reached on 571-272-4195. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Daniel L. Hoang/

Examiner, Art Unit 2436

/Nasser G Moazzami/

Supervisory Patent Examiner, Art Unit 2436